App. Ser. No. 09/992,580
Atty. Dkt. No. MIO 0072 VA

IN THE SPECIFICATION

Please delete the paragraph beginning at page 1, line 4.

Please replace the paragraph beginning at page 1, line 7 with the following replacement paragraph:

---This application is a division of U.S. Patent Application Serial No. 09/804,421 DIE STACKING SCHEME, filed March ~~12~~,30 2001, now U.S. Patent No. 6,441,483, issued August 27, 2002. This application is also related to U.S. Patent Application Serial Nos. 09,855,731, filed May 15, 2001; 09/804,051, filed March 12, 2001; 09/803,045, filed March 12, 2001; and 10/229,968 filed August 28, 2002.---

Please replace the paragraph beginning at page 10, line 22 with the following rewritten paragraph:

---In accordance with yet another embodiment of the present invention, a method of assembling a printed circuit board is provided. The method comprises the steps of: providing a substrate including a first surface and conductive contacts included on the first surface; providing a first semiconductor die including a pair of major surfaces, wherein one of the pair of major surfaces of the first die defines a first active surface, the other of the major surfaces of the first die defines a first stacking surface, and the first active surface includes a plurality of conductive bond pads; electrically coupling the first active surface to the substrate with a plurality of topographic contacts extending from respective conductive bond pads on the first active surface to corresponding conductive contacts on the first surface of the substrate; providing a second semiconductor die including a pair of major surfaces, wherein one of the pair of major surfaces of the second die defines a second active surface, the other of the major surfaces of the second die defines a second stacking surface, the second active surface includes a plurality of conductive bond pads, and the first stacking surface is devoid of conductive bond pads; securing the first stacking surface to the second stacking surface; securing a single decoupling capacitor to the second ~~stacking~~ active surface; providing a pair of conductive

lines, each of the conductive lines connecting a terminal of the decoupling capacitor, a bond pad on the second active surface, and a conductive contact on the first surface of the substrate; electrically coupling the conductive contact on the first surface of the substrate to the first semiconductor die via one of the plurality of topographic contacts extending from respective conductive bond pads on the first active surface to corresponding conductive contacts on the first surface of the substrate; arranging the pair of conductive lines such that the decoupling capacitor is connected across V_{ss} and V_{cc} pins of the first and second semiconductor dies; positioning a printed circuit board such that a first surface of the printed circuit board faces the substrate; and providing a plurality of topographic contacts extending from the substrate to the first surface of the printed circuit board.---